



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,313	06/30/2000	Gerolf F. Hoflehner	042390.P8132	9388

7590 02/13/2003

Robert B O'Rourke  
Blakely Sokoloff Taylor & Zafman LLP  
12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, CA 90025-1026

[REDACTED] EXAMINER

SHRADER, LAWRENCE J

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/608,313	HOFLEHNER ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Lawrence Shrader	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
 THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 6/30/2000.
- 2a) This action is FINAL.                  2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-67 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-67 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

- 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

Art Unit: 2124

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 11 – 16, 19 - 20, 23 - 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scales et al., U.S. Patent 5,950,228 (hereinafter referred to as Scales) in view of Orr, U.S. Patent 5,748,963.

Scales discloses a system in which allocation instructions are inserted in a program (column 17, lines 7 – 12), but does not teach the identification of a function call as the cause of the insertion. Orr, however, does teach the determination of a function call in a code segment (column 7, lines 42 – 45). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the function call identification method of Orr with the insertion of allocation instructions taught by Scales in order to insert allocation instructions in a routine if a function call instruction is found so that other resources, e.g., memory, registers, stacks, etc. might be allocated.

In reference to claim 11, official notice is taken for allocation of an instruction inserted just before the function-call because one of ordinary skill would expect that the proper allocation configuration be made before the function runs. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to insert an allocation instruction before the

function call so that the allocation of resources for the function is complete before the function is run.

In reference to claims 12 and 13, official notice is taken for allocation of an instruction inserted before the function-call because one of ordinary skill would expect that the proper allocation configuration be made before the function runs. Also, a pre-dominator block implies a dominator block, which in turn implies that a post-dominator block exists, i.e., a block being dominated. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to insert an allocation instruction before the function call, whether or not in a pre-dominator block, so that the allocation of resources is complete before the function is run.

In reference to claim 14, rejected for the same reasons put forth in the rejection of claim 1. Claim 14 would simply multiply the insertion of allocation instructions whenever a functional characteristic is found after searching. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to search for multiple functional characteristics and apply the allocation instruction insertions in order that each functional routine or block of code might contribute to the greater efficiency of the program.

In reference to claims 15,19, and 23, rejected for the same reasons put forth for claim 1. A functional characteristic corresponding to either a loop in a control flow graph, or a software pipelined loop may be interpreted as a routine resulting from a function call. In the case of a loop, a section of code need not be repeated as inline code; in the case of a software pipelined loop, the function may utilized so that the code might be optimized for greater throughput.

In reference to claims 16 and 20, rejected for the same reason put forth in the rejection of claim 11.

In reference to claim 24, official notice is taken that one cannot determine the number of registers to be allocated before the functional characteristic is known. Therefore it would have been obvious to one skilled in the art at the time the invention was made to determine the number of registers to be allocated for an allocation instruction after the functional characteristic was known so that the number of registers might than be determined.

Claims 2, 8, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scales et al., U.S. Patent 5,950,228 (hereinafter referred to as Scales) in view of Orr, U.S. Patent 5,748,963, and further in view of Proebsting et al., "Demand Driven Register Allocation" (hereinafter referred to as Proebsting).

In reference to claim 2, Scales discloses allocation instructions, and Orr teaches the determination of a function call in a routine. Neither Scales nor Orr teaches allocation for only live information, but Probsting teaches the allocation of registers for live information (page 683, Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the disclosures of Scales and Orr in order to insert allocation instructions in a routine if a function call instruction is found and to further modify the combination with the use of live data as taught by Proebsting so that only useful information is stored.

In reference to claim 8, Proebsting teaches local values to allocate registers to the given routine (page 1, Abstract) as applied to claim 2.

In reference to claim 9, Scales discloses allocation instructions, and Orr teaches the determination of a function call in a routine. Neither Scales nor Orr teaches a register space partitioned for global variables and one for local variables with said instruction allocating local

Art Unit: 2124

register space. Proebsting teaches the allocation of both local and global registers (page 1, Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to construct an allocation instruction according to the combination of Scales and Orr and further implement the instruction with the ability to partition register space for local variables, while allocating global registers by another means, as taught by Proebsting.

In reference to claim 10, Scales discloses allocation instructions, and Orr teaches the determination of a function call in a routine. Neither Scales nor Orr teaches allocation for live information that is global information, but Proebsting teaches the allocation of registers for global live information (page 1, Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the function call identification method of Orr with the insertion of allocation instructions taught by Scales in order to insert allocation instructions in a routine if a function call instruction is found, and further modified by Proebsting to include live variable information that is global so that a single register might be allocated for several variables that are not simultaneously live.

Claims 3 – 7, 17 – 18, 21 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scales et al., U.S. Patent 5,950,228 (hereinafter referred to as Scales) in view of Orr, U.S. Patent 5,748,963, further in view of Proebsting et al., “Demand Driven Register Allocation” (hereinafter referred to as Proebsting), and further in view of Srivastava, U.S. Patent 5,999,737.

In reference to claims 3 - 4 and 6 Scales discloses allocation instructions, and Orr teaches the determination of a function call in a routine; Proebsting teaches the allocation of live information for both local and global registers. None specifically teach the method of determining live information by identifying information that is referred to before and after a

function call (claim 3) and extending to the exit block of the routine (claim 4) or a post-dominator block (claim 6) - it is understood that a function call extending to an exit block would apply as well to a post-dominator block since the type of graph would not alter the method. Srivastava, on the other hand, teaches a liveness analysis wherein a set of live variables is determined at the beginning of execution of a function call and also at the end of the function call (column 8, lines 6 – 12); the liveness analysis also extends to the exit block, or a post-dominator, of the routine (10, lines 12 – 26). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to insert an allocation instruction as determined by the combination of the disclosures of Scales and Orr, and configuring the instruction to allocate only live information as modified by Srivastava, where said information is referred to both before and after a function call, and where the identified information extends to an exit block of the routine also taught by Srivastava so that resources are efficiently allocated for only useful data, and for increasing the efficiency of the compiled program.

In reference to claims 5 and 7, official notice is taken that none of the cited references work specifically to eliminate a worst-case path, therefore one may infer that the worst-case path may be allocated, especially in Probsting and Srivastava.

In reference to claims 17 and 21, rejected for the same reason put forth in the rejection of claim 5.

In reference to claims 18, rejected for the same reason put forth in the rejection of claim 7.

In reference to claim 22, rejected for the same reason put forth in the rejection of claim 6.

Claims 25 – 26 are rejected in line with the reasoning for claim 24. Functional characteristics must be known before a determination of a consequent action can be made.

Art Unit: 2124

In reference to claim 27, official notice is taken that building an understanding of a flow control graph is inherent in a compiling procedure, therefore searching could not be done prior to the understanding.

Claims 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Scales et al., U.S. Patent 5,950,228 (hereinafter referred to as Scales) in view of Orr, U.S. Patent 5,748,963, further in view of Proebsting et al., "Demand Driven Register Allocation" (hereinafter referred to as Proebsting), and further in view of Wu, U.S. Patent 6,230,317, and further in view of Aho et al., "Compilers" (hereinafter referred to as Aho).

a) performing a first allocation... Scales discloses allocation instructions, and Orr teaches the determination of a function call in a routine. Neither teaches the allocation of register space at the entry block of a routine. Aho teaches register allocation where code is generated for each block (section 9.7, p. 544), which could include an entry block. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the teachings of Scales and Orr to provide an allocation means, and further modify this means to allocate a first amount of register at the entry block as taught by Aho so that ample register space is allocated for the entire block..

b) *performing a second allocation...* rejected for the reason put forth in the rejection of claim 2.

c) *performing a function call...* rejected for the reason put forth in the rejection of claim 1.

d) *performing a third allocation...* Scales discloses allocation instructions, and Orr teaches the determination of a function call in a routine. Aho teaches register allocation at the

Art Unit: 2124

entry block where code is generated for each block. Neither Scales nor Orr nor Aho teaches the allocation of register space having a common register. Wu, on the other hand, teaches register allocation that has shared registers. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the teachings of Scales and Orr to provide an allocation means, modified by Aho to allocate a first amount of register space at the entry block, and further modified by Wu so that register spaces share a common register.

In reference to claims 29 – 33, rejected for the same reasons put forth for claims 3 – 7.

In reference to claims 34 – 36, rejected for the same reasons put forth in the rejection of claim 9.

In reference to claim 37, rejected for the same reason put forth in the rejection of claim 11.

In reference to claim 40, rejected for the same reasons put forth for claim 27.

Claims 41 – 53 (the medium) are rejected for the same reasons put forth for claims 1 – 13 (the method).

Claims 54 – 67 (the medium) are rejected for the same reasons put forth for claims 14 – 27 (the method).

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent 6,029,005 to Radigan, a compiling method inserting a phi function for a global variable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence Shrader whose telephone number is (703) 305-8046. The examiner can normally be reached on M-F 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Lawrence Shrader  
Art Unit 2124

February 10, 2003

*Lawrence Shrader*

KAKALI CHAKI  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100